CS152 Fall 2003
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HW3 Solutions

Version 1.0 – updated 10/26/2003
Email cs152-td@cory with corrections or questions.

7.7

1 miss, 4 miss, 8 miss, 5 miss, 20 miss, 17 miss, 56 miss, 9 miss, 19 miss, 11 miss, 4 miss, 43 miss, 5 hit, 6 miss, 9hit, 17 hit

Tag	Cache block
1	17 hit
1	19
0	4
0	5 hit
0	6
3	56
0	9 hit
2	43

7.9

of bits required is :
(128+16+1)*4k=580k

7.11

For organization a, miss penalty is 16*(10+1)=176 cycles
For organization b, miss penalty is 4*(10+1)=44 cycles
For organization c, miss penalty is 4*10+4*4=56 cycles

7.15

AMAT = 1*2+0.05*20*2=4ns

7.16

AMAT=1.2*2+0.03*20*2=3.6ns
The AMAT is improved by 10% but double the size of the cache. Probably it is a good tradeoff.

7.18

x*(1+32-log2(x)-2+32)<=18*32*8*1024bits => x<=85595.6 => we need cache line log2(x)=16.38
so set cache line size is 2^16=64k , Thus 8 of 32Kx8bits SRAM will be used for cache data storage, which is 64k words. The # of tag bits is 32-16-2=14 bits. The tag and valid bit consumes 15bits*64k=32k*30bits, which needs 4 32kx8 bit SRAM.

7.23

One example is the following memory address references: Assuming that cache size is 16 , the address is word address and each cache block is one word.
1, 2, 17, 33, 1,2
for 2-way associative cache, 1 miss, 2 miss, 17 miss(kick out 1), 33 miss(kick out 2), 1 miss, 2 miss
for directed map cache, 1 miss , 2 miss, 17 miss(kick out 1), 33miss(kick out 17), 1 miss, 2 hit

7.27

CPI= CPI_{hit}+miss rate*miss penalty
For cache 1:
CPI=CPI_{hit}+4%*(6+1)+0.5*8%*(6+1)=2 =>CPI_{hit}=1.44

For cache 2:
CPI= CPI_{hit}+2%*(6+4)+0.5*5%*(6+4)=1.44+0.45=1.89

For cache 3:
CPI = CPI_{hit}+2%*(6+4)+0.5*4%*(6+4)=1.44+0.40=1.84

Cache 1 spends the most cycles on cache miss