CS152 – Computer Architecture and Engineering
Lecture 23 – Goodbye to 152

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Outline

- Review 152 material: what we learned
- Cal v. Stanford
- Your Cal Cultural Heritage
- Course Evaluations

CS152: So what's in it for me?

- In-depth understanding of the inner-workings of computers & trade-offs at HW/SW boundary
  - Insight into fast/slow operations that are easy/hard to implement in hardware (HW)
  - Out of order execution and branch prediction
- Experience with the *design process* in the context of a large complex (hardware) design.
  - Functional Spec --> Control & Datapath --> Physical implementation
  - Modern CAD tools
  - Make 32-bit RISC processor in actual hardware
- Learn to work as team, with manager (TA)
- Designer's "Conceptual" toolbox.

Conceptual tool box?

- Evaluation Techniques
- Levels of translation (e.g., Compilation)
- Levels of Interpretation (e.g., Microprogramming)
- Hierarchy (e.g, registers, cache, mem,disk,tape)
- Pipelining and Parallelism
- Static / Dynamic Scheduling
- Indirection and Address Translation
- Synchronous /Asynchronous Control Transfer
- Timing, Clocking, and Latching
- CAD Programs, Hardware Description Languages, Simulation
- Physical Building Blocks (e.g., Carry Lookahead)
- Understanding Technology Trends / FPGAs

Project Simulates Industrial Environment

- Project teams have 4 or 5 members in same discussion section
  - Must work in groups in “the real world”
- Communicate with colleagues (team members)
  - Communication problems are natural
  - What have you done?
  - What answers you need from others?
  - You must document your work!!!
  - Everyone must keep an on-line notebook
- Communicate with supervisor (TAs)
  - How is the team’s plan?
  - Short progress reports are required:
    - What is the team’s game plan?
    - What is each member’s responsibility?

Review: Week 1, Tu

- Continued rapid improvement in Computing
  - 2X every 1.5 years in processor speed; every 2.0 years in memory size; every 1.0 year in disk capacity; Moore's Law enables processor, memory (2X transistors/chip/ ~1.5 yrs)
- 5 classic components of all computers

Control Datapath Memory Input Output

Review: Week 2

- 4-LUT FPGAs are basically interconnect plus distributed RAM that can be programmed to act as any logical function of 4 inputs
- CAD tools do the partitioning, routing, and placement functions onto CLBs
- FPGAs offer compromise of performance, Non Recurring Engineering, unit cost, time to market vs. ASICs or microprocessors (plus software)

	Performance	*NRE*	*Unit Cost*	*TTM*
Better	ASIC	MICRO	ASIC	MICRO
	FPGA	FPGA	MICRO	FPGA
Worse	MICRO	ASIC	FPGA	ASIC

Performance Review: Week 3

- Latency v. Throughput
- Performance doesn't depend on any single factor: need to know Instruction Count, Clocks Per Instruction and Clock Rate to get valid estimations
- 2 Definitions of times:
  - User Time: time user needs to wait for program to execute (multitasking affects)
  - CPU Time: time spent executing a single program: (no multitasking)
- Amdahl's Law: law of diminishing returns

Review Single Cycle Datapath: Week 4

- 5 steps to design a processor
  1. Analyze instruction set => datapath requirements
  2. Select set of datapath components & establish clock methodology
  3. Assemble datapath meeting the requirements
  4. Analyze implementation of each instruction to determine setting of control points that effects the register transfer.
  5. Assemble the control logic
- MIPS makes it easier
  - Instructions same size; Source registers, immediates always in same place
  - Operations always on registers/immediates
- Single cycle datapath => CPI=1, CCT => long
- On-line Design Notebook
  - Open a window and keep an editor running while you work;cut&paste
  - Former CS 152 students (and TAs) say they use on-line notebook for programming as well as hardware design; one of most valuable skills
  - Refer to the handout as an example

Review multicycle processor: week 5

- Control is specified by finite state diagram
- Specialized state-diagrams easily captured by microsequencer
  - simple increment & “branch” fields
  - datapath control fields
- Control is more complicated with:
  - complex instruction sets
  - restricted datapaths (see the book)
- Control design can become Microprogramming

Review Pipelining: Week 6

- Reduce CPI by overlapping many instructions
  - Average throughput of approximately 1 CPI with fast clock
- Utilize capabilities of the Datapath
  - start next instruction while working on the current one
  - limited by length of longest stage (plus fill/flush)
  - detect and resolve hazards
- What makes it easy
  - all instructions are the same length
  - just a few instruction formats
  - memory operands appear only in loads and stores
- What makes it hard?
  - structural hazards: suppose we had only one memory
  - control hazards: need to worry about branch instructions
  - data hazards: an instruction depends on a previous instruction

Review Cache: Week 8

- Two Different Types of Locality:
  - Temporal Locality (Locality in Time): If an item is referenced, it will tend to be referenced again soon.
  - Spatial Locality (Locality in Space): If an item is referenced, items whose addresses are close by tend to be referenced soon.
- SRAM is fast but expensive and not very dense:
  - 6-Transistor cell (no static current) or 4-Transistor cell (static current)
  - Does not need to be refreshed
  - Good choice for providing the user FAST access time.
  - Typically used for CACHE
- DRAM is slow but cheap and dense:
  - 1-Transistor cell (+ trench capacitor)
  - Must be refreshed
  - Good choice for presenting the user with a BIG memory system
  - Both asynchronous and synchronous versions
  - Limited signal requires “sense-amplifiers” to recover

Review: Week 9

- Superpipelined
- Superscalar
- Very Long Instruction Word machines (VLIW)
  $\Rightarrow$ Multiple operations coded in single, long instruction
  - Requires sophisticated compiler to decide which operations can be done in parallel

Review: Week 10

- Reservations stations: renaming to larger set of registers + buffering source operands
  - Prevents registers as bottleneck
  - Avoids WAR, WAW hazards of Scoreboard
  - Allows loop unrolling in HW
- Not limited to basic blocks (integer units gets ahead, beyond branches)
  - Dynamic hardware schemes can unroll loops dynamically in hardware
  - Dependent on renaming mechanism to remove WAR and WAW hazards
- Helps cache misses as well

Review: Week 11

- **Reorder Buffer:**
  - **Provides generic mechanism for "undoing" computation**
  - **Instructions placed into Reorder buffer in *issue order***
  - **Instructions exit in same order – providing *in-order-commit***
  - **Trick: Don't want to be canceling computation too often!**
- **Branch prediction important to good performance**
  - **Depends on ability to cancel computation (Reorder Buffer)**
- Explicit Renaming: more physical registers than ISA.
  - **Separates *renaming* from *scheduling***
    - **Opens up lots of options for resolving RAW hazards**
  - **Rename table: tracks current association between architectural registers and physical registers**
  - **Potentially complicated rename table management**
- Parallelism hard to get from real hardware beyond today

Review Road to Faster Processors: Week 12

- Time = Instr. Count x CPI x Clock cycle time
- How get a shorter Clock Cycle Time?
- Can we get CPI < 1?
- Can we reduce pipeline stalls for cache misses, hazards, … ?
- IA-32 P6 microarchitecture (μarchitecture): Pentium Pro, Pentium II, Pentium III
- IA-32 "Netburst" μarchitecture (Pentium 4, …
- IA-32 AMD Athlon, Opteron μarchitectures
- IA-64 Itanium I and II microarchitectures

Review Buses and Networks: Week 13

- Buses are an important technique for building large-scale systems
  - Their speed is critically dependent on factors such as length, number of devices, etc.
  - Critically limited by capacitance
- Direct Memory Access (dma) allows fast, burst transfer into processor's memory:
  - Processor's memory acts like a slave
  - Probably requires some form of cache-coherence so that DMA'ed memory can be invalidated from cache.
- Networks and switches popular for LAN, WAN
- Networks and switches starting to replace buses on desktop, even inside chips

Week 14: Bandwidth Yes, Latency No

Technology	Bandwidth / Year	Latency / Year	Capacity / Year
Networks	80%	15%	n.a.
Disks	30%	10%	100%
DRAM	30%	5%	40%
Processors	70% (MIPS)	20%	n.a.

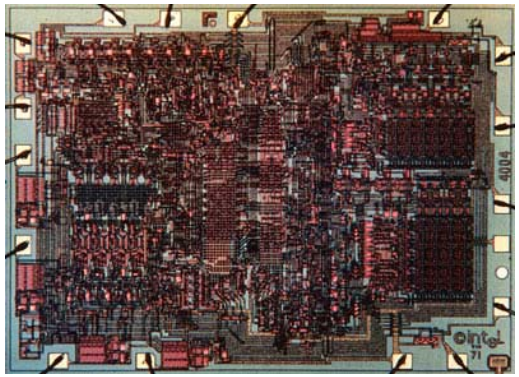
- Annual % BW = 4 (+–2) x Annual % latency
- Innovators should bet on advances in bandwidth vs. latency

MultiThreaded Categories

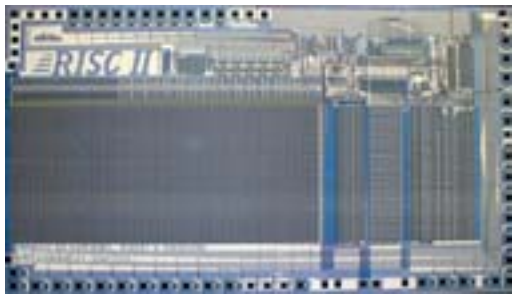
(Slide from Jun Yang, U.C.R., Winter 2003)

Long Term Challenge: Micro Massively Parallel Processor (μMMP)

- Intel 4004 (1971): 4-bit processor, 2312 transistors, 0.4 MHz, 10 micron PMOS, 11 mm^2 chip



- RISC II (1983): 32-bit, 5 stage pipeline, 40,760 transistors, 3 MHz, 3 micron NMOS, 60 mm^2 chip
  - 4004 shrinks to ~ 1 mm^2 at 3 micron

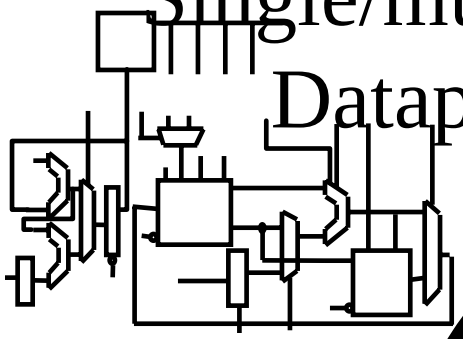


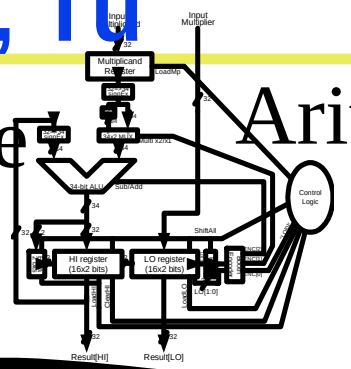
- 250 mm^2 chip, 0.090 micron CMOS = 2312 RISC IIs + Icache + Dcache
  - RISC II shrinks to ~ 0.05 mm^2 at 0.09 mi.
  - Caches via DRAM or 1 transistor SRAM (www.t-ram.com)
  - Proximity Communication via capacitive coupling at > 1 TB/s (Ivan Sutherland@Sun)
  - Processor = new transistor?

Cost of Ownership, Dependability, Security v. Cost/Perf. => μMPP

Review: Week 1, Tu

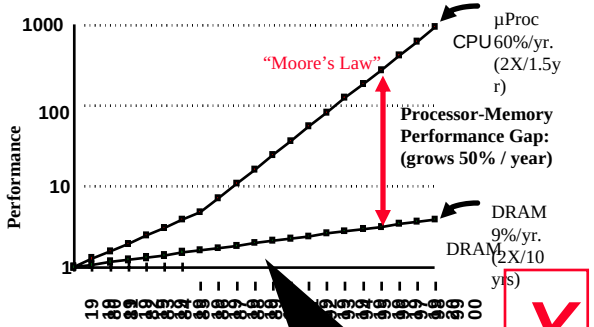
Single/multicycle Datapaths

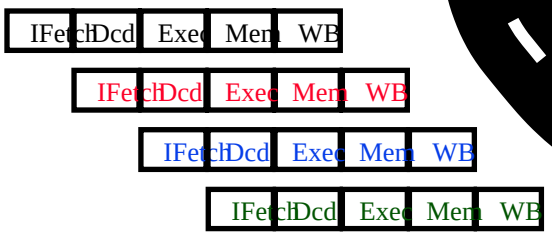




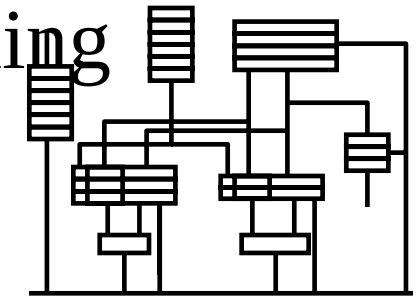
Arithmetic

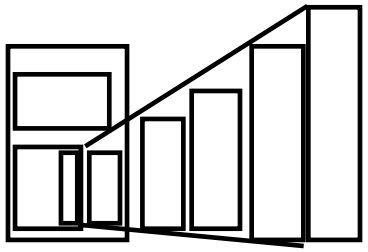
CS152 Fall '03

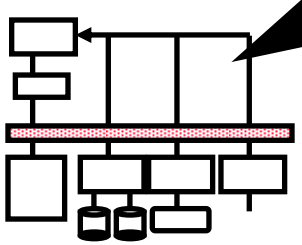




Pipelining







I/O

Memory Systems

YOUR CPU

Xilinx Field Trip

- FPGA: simple block, replicated many times
  - Early user of new technology (90 nm v. 130)
  - Easy to make many different sized chips with very different costs: $10 to $5000
  - Follows Moore's Law to get more on chip
- Spin FPGA design into ASIC?
  - No technical obstacles, just requires designer constraint to select compatible blocks
  - But no business reason to make it easy since Xilinx doesn't sell ASIC chips or services
- Future: FPGA as "system on a chip" vehicle?
  - SRAM dependability at 60 nm? 25 nm?

Opportunity to Improve Future 152 classes?

- Learn to write good English by reading good books; learn to write good Verilog by studying good designs?
- Interested in converting VHDL MicroBlaze to Verilog as an Intern at Xilinx? (1 month?)
- Interested in converting advanced MIPS design to Verilog as an Intern at MIPS?

Things we Hope You Learned from 152

° Keep it simple and make it work:

- Fully test everything individually & then together; break when together
- Retest everything whenever you make any changes
- Last minute changes are big “no nos”

° Group dynamics. Communication is key to success:

- Be open with others of your expectations & your problems
- Everybody should be there on design meetings when key decisions are made and jobs are assigned

° Planning is very important (“plan your life; live your plan”):

- Promise what you can deliver; deliver more than you promise
- Murphy’s Law: things *DO* break at the last minute
  - *DON’T* make your plan based on the best case scenarios
  - Freeze your design and don’t make last minute changes

° Never give up! It is not over until you give up
(“Don’t fall with the ball”)

Outline

- Review 152 material: what we learned
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- Your Cal Cultural Heritage
- Course Evaluations

CompSci B.S.: Cal vs. Stanford

- 97/98 Degrees: 242 (Cal) v. 116 (Stanford)
  - Cal: L&S Computer Science + EECS Option C
  - Stanford: Computer Science (C.S. Dept.) + Computer Systems Engineering (E.E. Dept.) + Symbolic Systems (Interdepartmental)
- Cal 2.1X Stanford in CompSci degrees/year
- Gordon Moore, Intel founder (Moore's Law): "Lots more people in Silicon Valley from Cal than from Stanford"
- Apply 61C Big Ideas to Life!
  Cal v.Stanford Cost-Performance Benchmark

Cal v. Stanford Cost-Performance

- Cost is easy:
  - Tuition (or Tuition + Room & Board) * 4.5 years
- Performance?
  - Independent Anecdotal Comments
  - Industry salary for B.S. in C.S.
  - Programming contest results
  - Computing Research Awards to Undergrads
  - Ph.D. programs: prefer Cal or Stanford alumni
  - (Your good idea goes here)

Cost: Cal vs. Stanford CS Degrees

- Cost Benchmark (2003- 2004 costs)
- Tuition: $28,563 (Stanford) v. $5,858 (Cal)
  - Cal cheaper by factor of 4.9X
  - Save $22,700 / year
  - (Out-of-state tuition $20,068, 1.4X, save $8k/yr)
- 4.5 years * Tuition + Room & Board
- Stanford Cost: 4.5 * $36,857 = $165,902
- Cal Cost: 4.5 * $14,353 = $64,588
  - Cal cheaper by 2.6X, save $100,000 (1.3X, $40k)

Source: http://registrar.berkeley.edu/Registration/feesched.html
http://www.stanford.edu/dept/registrar/registration/tuition.html

Anecdotal Qualitative Assessments

- Intel recruiter, several others companies "Cal B.S. degree is equivalent to a Stanford M.S. degree"
- HP VP: point new college hire to desk, tell where computers located

Next day, Cal alumni:
O.S. installed, apps installed, computer on network, sending email, working away

- "Can do" attitude

Next day, Stanford alumni:
"When will someone setup my computer?"

"Can't do" attitude

Going to Industry: Salary

- 2001-2002 Starting Salaries B.S. in CS (according to each Placement center)
- Stanford: median $60,800 (10 people)
- Cal: median $60,000 (20 people)
- Assuming sample size sufficient, Stanford starting salary is within 1% of Cal starting salary

Sources: http://career.berkeley.edu/Major2002/CompSci.stm

http://www.stanford.edu/dept/CDC/surveys/0102/engineering.html

ACM Programming Contests: Last decade

Year	Regional	International
93/94	1. , 5. Cal, 6. Stanford	6. Cal, dnc St.
94/95	1. Cal, 2. Stanford	2. Cal, 19. St.
95/96	1. Cal, 5. Stanford	1. Cal, dnc St.
96/97	2. Stanford, 4. Cal	16. St., dncCal
97/98	1. Stanford, 2. Cal	11. Cal, 24 St.
98/99	1., 4. Cal, 2., 3. Stanford	7. Cal, 40 St.
99/00	1., 2. Stanford, 7., 8, 16. Cal	15. St.,dncCal
00/01	1. Cal, 2. Stanford	14 St., 29. Cal
01/02	1. Stanford, 2, 3, 4: Cal	5. St., 41 Cal
02/03	2, 8. Cal; 5, 6, 10 Stanford	13 Cal, dnc St.
03/04	dnc Cal; 2, 5 Stanford	?? St, dncCal

- Regional: Cal wins 5/10 years, Stanford 3/10 yrs
- Interntational: Cal won once, 6/11 times ahead of Stanford

Sources: http://www.acmcontest-pacnw.org/

http://icpc.baylor.edu/past/default.htm

CRA Outstanding Undergraduate Awards

- Started 1995, by Computing Research Association
- 2 Nominations / school / year: 2 Winners, few Runners Up, many Honorable Mentions
  - Total: 16 winners, 30 Runners Up, >200 Hon. Men.
- Number winners Total Named Points (3/2/1)

40. Stanford (0)	22. Stanford (3)	22. Stanford (3)
5. MIT (1)	14. MIT (3)	11. MIT (5)
1. Dartmouth (2)	3. Cornell (8)	3. Dartmouth (14)
1. Harvard (2)	2. Harvard (10)	2. Harvard (16)
1. Cal (2)	1. Cal (20)	1. Cal (25)

Going on to Ph.D. in C.S.

- 1997: ~ 25% of Cal EECS students go on for PhD,
  <5% of Stanford students go for PhD

Fall 1999 applicants	Undergraduate Alma Mater		
Grad School Admit	Stanford	Cal	Ratio
Univ. Washington	5	7	1.4
MIT	3	6	2.0
Carnegie Mellon	1	4	4.0
Stanford	??	6	?
Cal	0	8	∞

B I G 4

Summary of Cost-Performance Comparison

- Can Apply Computer Design to Life!
- Cost: Cal 2.4X better than Stanford
- Performance:
  - Cal = Stanford starting salary
  - Cal > Stanford: programming contests, undergrad awards, PhD attractiveness, anecdotal quality assessment
- Cost-Performance: Cal is best by far; Is there a second place?

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What to Emphasize about Cal culture?

- Top public university for undergraduate education? (US News)
- Top graduate program, public or private, in the world? (35/36 departments in the top 10; National Research Council)
- Faculty Awards?
  - 8 current Nobel Prize winners (18 all time)
  - 19 current "Genius" awards winners (MacArthur fellows)
  - 85 in National Academy of Engineering
  - 124 in National Academy of Science
  - Source: `http://www.berkeley.edu/about/honors/`

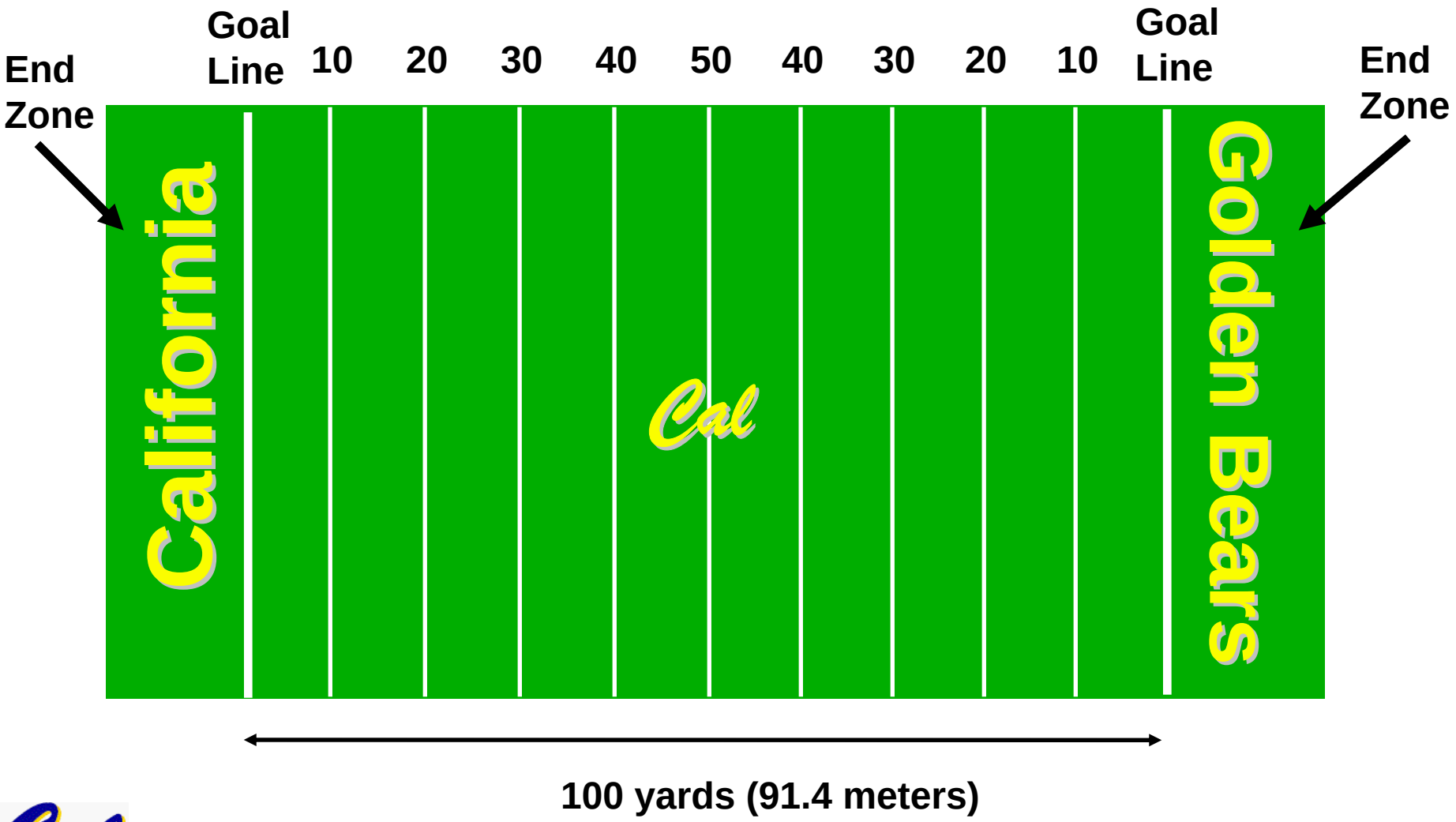
Cal Cultural History: ABCs of Football

- Started with “soccer”; still 11 on a team, 2 teams, 1 ball, on a field; object is to move ball into “goal”; most goals wins. No hands!
- New World changes rules to increase scoring:
  - Make goal bigger! (full width of field)
  - Carry ball with hands
  - Can toss ball to another player backwards or laterally (called a “lateral”) anytime and forwards (“pass”) sometimes
- How to stop players carrying the ball? Grab them & knock them down by making knee hit the ground (“tackle”)

ABCs of American Football

- **Score by...**
  - **moving football into goal ("cross the goal line" or "into the end zone") scoring a "touchdown" (6 points)**
  - **kicking football between 2 poles ("goal posts") scoring a "field goal" (worth 3 points, unless after touchdown, then its just 1 point: "extra point")**
- **Kick ball to other team after score ("kickoff")**
  - **laterals OK**
- **Game ends when no time left (4 15 min quarters) and person with ball is stopped (Soccer time only: 2 45 min halves, time stops play)**

Football Field



The Spectacle of American Football

- Cal's archrival is Stanford
  - stereotype is Private, Elitist, Snobs
- Play nearby archrival for last game of season
  - Called "The Big Game": Cal vs. Stanford, winner gets a trophy ("The Axe") : Oldest rivalry west of Mississippi; 100th in 1997
- American college football is a spectacle
  - School colors (Cal Blue & Gold v. Red & White)
  - Nicknames (Golden Bears v. Stanford Cardinal)
  - School mascot (Oski the bear v. a tree(!))
  - Leaders of cheers ("cheerleaders")

The Spectacle of American Football

- "Bands" (orchestras that march) from both schools at games
- March & Play
  - before game, at halftime, after game
- Stanford Band more like a drinking club; (Seen the movie "Animal House"?)
  - Plays one song: "All Right Now"
  - Cannot march and play

1982 Big Game

"There has never been anything in the history of college football to equal it for sheer madness."

"Top 20 favorite sports event in 20th century", *Sports Illustrated*

"The Greatest Display of Teamwork in the History of Sport" *Several sportswriters*

"…The Play, widely considered the most dramatic ending in college football history" , AP news

- **Stanford**
  - **Quarterback is John Elway, who goes on to be a professional All Star football player (retired 1999) Possibly greatest quarterback in college history?**
    - **In 1982, they had lost 4 games in last minutes**
- **Stanford has just taken lead with 4 seconds left in game; Cal team captain yells in huddle "Don't fall with the ball!"; watch video**

Notes About "The Play" (1/3)

"Allright here we go with the kick-off. Harmon will probably try to squib it and he does. Ball comes loose and the Bears have to get out of bounds. Rogers along the sideline, another one... they're still in deep trouble at midfield, they tried to do a couple of....the ball is still loose as they get it to Rogers. They get it back to the 30, they're down to the 20...Oh the band is out on the field!! He's gonna go into the endzone!!! He got into the endzone!! …
THE BEARS HAVE WON!!! THE BEARS HAVE WON!!! Oh my God, the most amazing, sensational, dramatic, heart rending... exciting thrilling finish in the history of college football!"
– KGO's Joe Starkey

Notes About "The Play" (2/3)

- Cal only had 10 men on the field; last second another came on (170 pound Steve Dunn #3) and makes key 1st block
- Kevin Moen #26: 6'1" 190 lb. safety,
  - laterals to Rodgers (and doesn't give up)
- Richard Rodgers #5: 6' 200 lb. safety, Cal captain "Don't fall with that ball."
  - laterals to Garner
- Dwight Garner #43: 5'9" 185 lb. running back
  - almost tackled, 2 legs & 1 arm pinned, laterals
- Richard Rodgers #5 (again): "Give me the ball!"
  - laterals to Ford

Notes About "The Play" (3/3)

- **Mariet Ford #1: 5'9", 165 pound wide receiver**
  - **Smallest player, leg cramps; overhead blind lateral to Moen and blocks 3 players**
- **Moen (again) cuts through Stanford band into end zone (touchdown!), smashes Trombonist**
- **On field for Stanford: 22 football players, 3 Axe committee members, 3 cheerleaders, 144 Stanford band members (172 for Stanford v. 11 for Cal)**
  - **"Weakest part of the Stanford defense was the woodwinds." -- Cal Fan**
- **Cal players + Stanford Trombonist (Gary Tyrrell) hold reunion every year at Big Game; Stanford revises history (20-19 on Axe)**

2003 Big Game: Cal 28 to 16 over Stanford

Penultimate slide: Thanks to the TAs

- John Gibson
- Jack Kang
- Kurt Meinz

The Future for Future Cal Alumni

- What's The Future?
- New Millennium
  - Internet, Wireless, Nanotechnology, Computational Biology, Rapid Changes ...
  - World's Best Education
  - Hard Working / Can do attitude
  - Never Give Up ("Don't fall with the ball!")

"The best way to predict the future is to invent it" – Alan Kay

Future is up to you!